DIGITAL RADIO LINK SYNTHESIZED WITH A DIRECT-DIVISION PLL AT 22 GHz

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ABSTRACT

An innovative 22 GHz digital multi channel has been prototyped to be used in urban areas where the communication link between computers, PABX, etc..., is essential. Low costs have been achieved by integration of the RF head into a single microstrip assembly. High stability oscillators through a direct-division phase-lock loop at 22 GHz, is the most outstanding feature of our prototype.

I. INTRODUCTION

In the last few years a sequence of technologies has been developed very successfully as far the reliabilty, capacity and economy of communication systems are concerned.

This has been particulary noticed in the progressive usage of many telecommunications' services. Therefore, it is necessary to develop wide-band distributing local networks in which transmission via radio is more efficient in networks of easy and fast installation, providing that the distance between terminals is comparatively small.

In this paper, a novel radio subsystem will be presented. It is a SHF (21.2-23.6 GHz) digital multi channel link with a transmitting data speed of 2.048 Mbit/s (30 PCM). This equipment has been mainly developed for short hops in urban areas where the communication links, between computers, PABX, etc.., are essential in large companies.

Several systems have been previously presented (1), (2), but our prototype presents the innovation of obtaining high frequency stability of transmitter and local oscillators by a direct-division phase-lock loop at 22 GHz.

II. MAIN FEATURES OF THE SYSTEM

The main features of the system are shown in table I.

The system's noise figure (12 dB) makes it possible to obtain a receiver sensitivity of -86 dBm with a 3.5 MHz filter and 2 FSK modulation. The values of output power and aerial's gain, permit an available gain of the system of 184 dB which assures a transmission range of 10 Km for a rainfall outage of less than 0.01% average per year for the worst Spanish weather conditions.

Table I. System parameters

Frequency band	21.2-23.6 GHz
Output power	18 dBm
Antenna gain	40 dBi
Noise figure	12 dB
Modulation	2FSK
Frequency stability	$\pm 1.10^{-6}$ p/d
Receiver sensibility: thermal noise, 35 MHz BW + noise figure + required C/N at 1 in 10^{-3} BER	-86 dBm
Available system gain	184 dB

Frequencies can be synthesized in 1.75 MHz paths by means of a PLL with direct frequency division.

III. SYSTEM DESCRIPTION

Figure 1 shows the block-diagram of the RF front-head whose physical realization can be seen in figure 2. Both transmitter and receiver microstrip circuits were made on Cu-Clad substrate of 2.17 relative constant and 0.127 mm. thick.

III.1 Transmitter

The transmitter is shown in figure 3. The power is generated by a dielectric oscillator with a gunn diode. It has a mechanical tunning of 0.5 GHz and output power greater than 22 dBm in the working frequency band. The oscillator is phase-locked by means of a loop which will be described later. Its output signal comes from a wave guide-microstrip transition and goes through a band-pass filter. The

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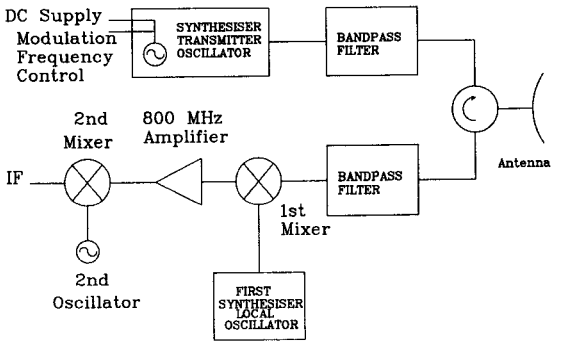

Figure 1. Block diagram of transceiver

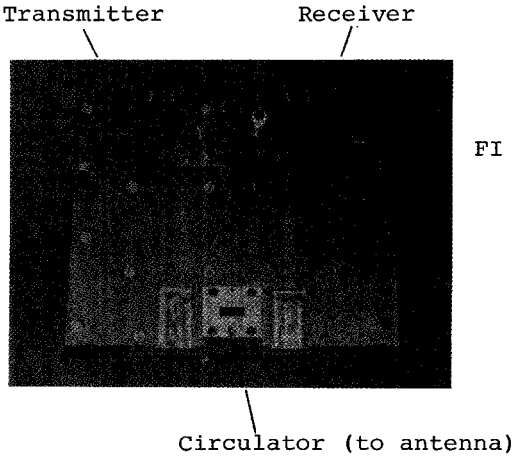

Figure 2. RF Front-Head

transition has a 0.5 dB loss. The bandpass filter is a plan-E with three cavities, it has a pass band of 300 MHz and less than 0.5 dB loss. Finally, the signal reaches the antenna through a waveguide circulator. The aerial is a 0.6 m. parabolic antenna which has 40 dBi gain.

III.2 Receiver

The receiver is shown in figure 4. The signal received by the antenna once separeted (diplexing circulator) from the transmitter goes throug a filter, of similar characteristics to the one described before, then through a waveguide-microstrip transition, before finally reaching the first mixer (3). It is simple balanced, using beam-lead schottky barrier diodes in a hybrid ring. The mixer has a conversion loss better than 7 dB and a noise figure better than 8

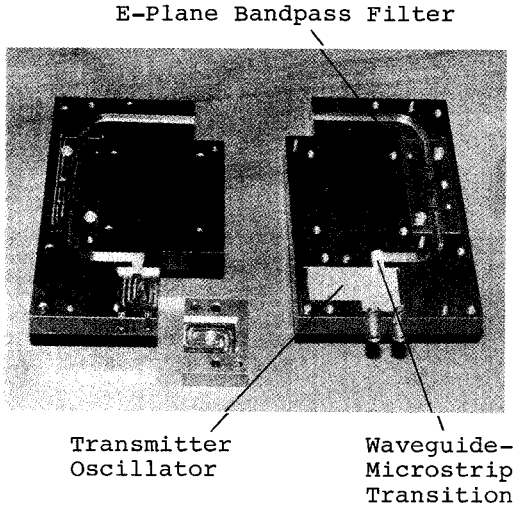

Figure 3. Picture of the transmitter

dB (single side band).

The first local oscillator is similar to the one used in the transmitter but uses a gunn diode with less output power. This oscillator delivers 15 dBm in its mechanical tunning range (500 MHz), and it is also stabilized by means of a PLL.

The first IF is 800 MHz. This IF signal goes through an amplifier of 30 dB gain and then is down-converted to a second IF signal of 35 MHz by means of a conventional mixer. A multiple-stage limiting amplifier, follows with a dynamic range of 60 dB for compensating fading and path variations. The base-band is then obtained by means of a delay line discriminator.

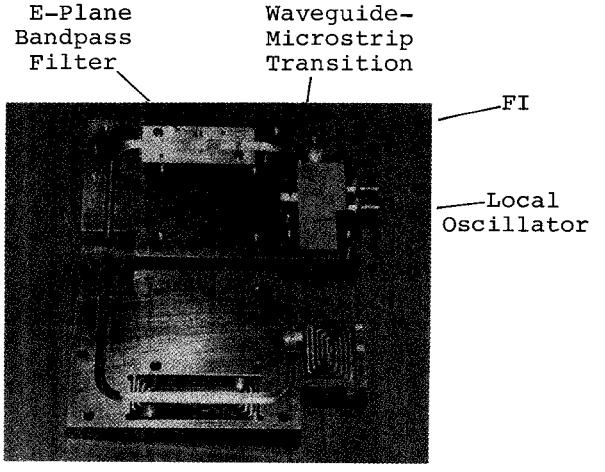

Figure 4. Picture of the receiver

III.3 Synthesizer with direct-division

Figure 5 shows the block-diagram of the synthesizer. Here we can see that the 22 GHz signal is divided by 12 (÷ 12) by a chain of analog dividers. Then a digital division is realized until a reference crystal is reached. The divider chain test fixture, including first digital divider and bias circuit, is shown in figure 6.

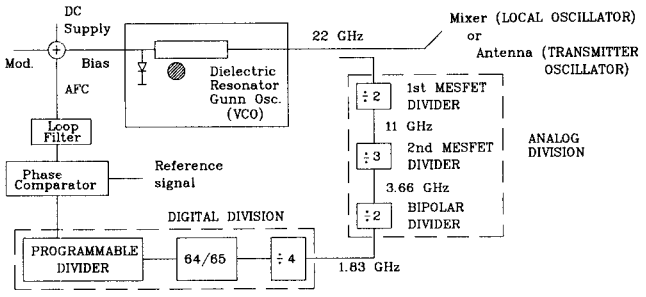

Figure 5. Block-diagram of the synthesizer

Direct division is obtained by analog dividers made with harmonic-injection locked oscillators. The first two dividers have been realized with MESFET, and the third one with a bipolar transistor. These dividers can be locked in a frequency range greater than 25% of the service band (21.2-23.6 GHz) between -15°C and 60°C, and is determinated by the first divider (from 22 GHz to 11 GHz). This locking range is larger than those refered to in specialized literature.

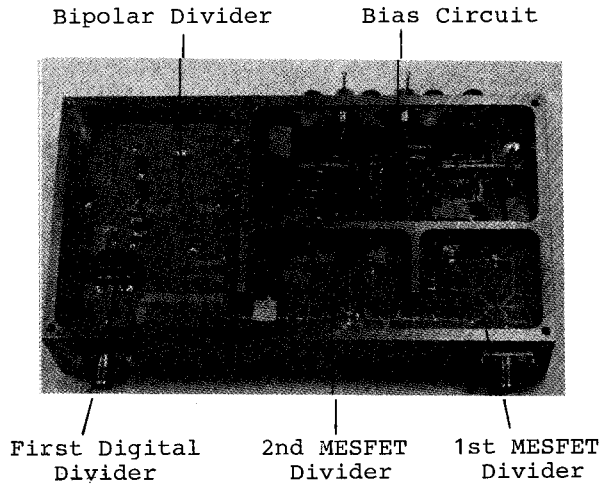

Figure 6. Divider chain test fixture

As can be seen in figure 6 all dividers were made on microstrip substrate of 2.17 relative constant, and 0.254 mm. thick.

The most critical divider was the first one by two (from 22 GHz to 11 GHz). The design procedure followed to make this divider can be resumed in the following steps:

1. Small signal matching of the active device and selection of an adequate bias point that gives an optimum trade-off solution between locking range and output power.
2. Calculation of the non-linear transfer function around the chosen bias point.
3. Design of the linear network that loads the matched device. This network should have a low-pass filter characteristic, a low Q and should permit oscillation at the point of maximum power of the unlocked device.
4. Free running oscillator analysis.
5. Calculation of the locking range.

The experimental results were as follows:

- locking range (from -15°C to 60°C): 300 MHz (2.7%)
- injection power: 5 dBm
- output power: > 0 dBm

More details on the design and performance of this divider and the other analog dividers can be found in references (4) and (5).

Digital division was made in the first step by a divider by 4 prescaler, and then we have the basic system of a single loop frequency synthesizer, where a 2-modulus prescaler (64/65) is used to divide the prescaler output frequency down to a suitable range for use in the CMOS device. This CMOS device contains the final programmable divider, as well as another one for the crystal reference frequency, and the phase detector.

The signal from the programmable divider is phase compared with the divided cristal (5.25 MHz) at reference frequency wich is 36.458 KHz so that frequencies can be synthesized as 22,000 $\pm$ n 1.75 MHz.

The error signal of the phase detector goes through an active loop filter, made with a low noise operational amplifier, and a drive-amplifier which drives the RF oscillator.

IV. CONCLUSIONS

A new low-cost, effective and reliable radio subsystem, working in the 21.2 - 23.6 GHz band, has been presented in this

Paper. Its most outstanding feature is the direct-division technique used in the synthesizer that the system incorporates.

V. ACKNOWLEDGEMENTS

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